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(54) Process for manufacture of micro electromechanical devices having high electrical isolation

(57) The present invention relates to a fabrication process for manufacture of micro electromechanical (MEM) devices such as cantilever support beams. This fabrication process requires only two lithographic masking steps and offers moveable electromechanical devices with high electrical isolation. A preferred embodiment of the process uses electrically insulating glass substrate (102) as the carrier substrate and single crystal silicon (108) as the MEM component material.

The process further includes deposition of an optional layer of insulating material (110) such as silicon dioxide on top of a layer of doped silicon (108) grown on a silicon substrate. The silicon dioxide (110) is epoxy

bonded to the glass substrate (102) to create a silicon-silicon dioxide-epoxy-glass structure (200). The silicon is patterned using anisotropic plasma dry etching techniques. A second patterning then follows to pattern the silicon dioxide layer (110) and an oxygen plasma etch is performed to undercut the epoxy film (120) and to release the silicon MEM component. This two-mask process provides single crystal silicon MEMs with electrically isolated MEM component. Retaining silicon dioxide insulating material (110) in selected areas mechanically supports the MEM component.

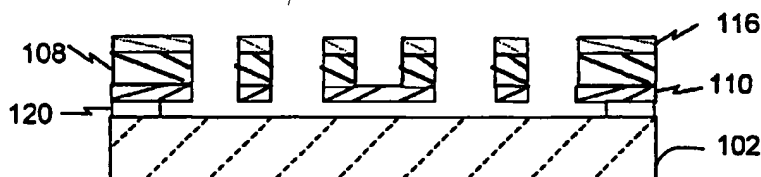


FIGURE 4

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## Description

### BACKGROUND OF THE INVENTION

#### (1) Field of the Invention

[0001] The present invention relates to micro electro-mechanical (MEM) systems and, more particularly, to fabrication of MEM components with a high electrically isolated substrate.

#### (2) Description of Related Art

[0002] Micro electromechanical (MEM) components are being progressively introduced into many electronic circuit applications and a variety of micro-sensor applications. Examples of MEM components are radio frequency (RF) switches, high Q capacitors, pressure transducers and accelerometers. One such MEM component, a MEM switch, is disclosed in U.S. Patent No. 5,578,976 which issued to Rockwell International Corporation the assignee of the present application. This MEM switch is fabricated on a GaAs substrate with a cantilevered switch arm formed from silicon dioxide-deposited upon a sacrificial layer. Contacts and electrodes are readily formed through deposition of gold and aluminum, respectively.

[0003] Another prior art method for creating cantilever beams required a deep anisotropic etch into a silicon substrate and application of either a silicon nitride or oxide layer to coat the top and side walls of the exposed cut. An isotropic etch of the silicon substrate undercuts and frees the MEM component. Unfortunately, this method is not readily adaptable for applications where non-conductive, high resistance substrates such as glass are desired for high isolation applications.

[0004] Another method, often referred to as a surface micro machining, uses a sacrificial layer such as silicon dioxide deposited on a silicon substrate. MEM component material, poly-silicon, by way of example, is then deposited, patterned and released. The poly-silicon layer is etched by a reactive ion etch to expose the sacrificial silicon dioxide layer. The sacrificial layer is then etched, usually with an acid (hydrofluoric acid), to release the MEM component. However, MEM components created from poly-silicon have limited mechanical strength and exhibit relatively poor electrical isolation. Further, production yields are poor using this method since the wet hydrofluoric etch often results in the MEM component sticking to the substrate rather than being suspended.

[0005] If a high electrical isolation is required, fabrication of MEM components on a glass substrate generally required either ionic (application of high voltage) or fusion (high temperature) bonding techniques to create MEM components. Both of these bonding techniques are poorly suited for use when semiconductor devices are present on the same substrate. Specifically, with

ionic bonding the high voltage may damage sensitive electrical components while the high processing temperature associated with both ionic and fusion bonding may cause junction depths to change affecting device performance and reliability. It is also known that such bonding techniques require very smooth surface to surface contact to ensure a good bond. If the surfaces do not mate within acceptable tolerances, the reaction or inter-diffusion process will result in a defective bond. Further, these bonding techniques are sensitive to surface contamination or irregularities which may result in bond failure sites or a decrease in production yields.

[0006] In another prior art method, a glass substrate is bonded to a silicon dioxide layer using ionic or fusion bonding techniques. Prior to bonding, the silicon dioxide layer is deposited on top of a silicon wafer so that the bonding process forms a glass-silicon dioxide-silicon composite structure. The silicon is patterned and wet etched to define the MEM component.

[0007] As mentioned above, ionic or fusion bonding require a high process temperature which are in the range of about 450°C to 500°C. Further, the glass substrate must be conductive to facilitate bonding with the silicon dioxide. Such conductivity precludes achieving high electrical isolation in the final MEM system. Further still, with the wet etch used to release the MEM component, the structure often sticks to the substrate rather than remaining free standing.

[0008] The present invention provides a method that uses adhesive bonding to form a MEM component on top of a glass substrate so that the MEM component is electrically isolated from the substrates. Further, the present process uses a dry etch to release the MEM component. Thus, whatever the merits of the above described prior art methods, they do not achieve the benefits of the present invention.

### SUMMARY OF THE INVENTION

[0009] The present invention relates to a fabrication process for manufacture of micro electromechanical (MEM) systems having components, such as cantilever supported beams, spaced above the substrate. This fabrication process uses as few as two lithographic masking steps depending on the complexity of the device and provides MEM components that are electrically isolated from the substrate.

[0010] Specifically, in one embodiment of the present invention, a composite silicon-film-glass substrate structure is formed. The silicon layer is processed by either polishing, grinding or etching to obtain the desired thickness, patterned to define the MEM component and etched to expose the film layer. The film layer is a sacrificial layer that is then patterned and dry etched to release the MEM component.

[0011] In other embodiment of the present invention, the process comprises the steps of growing a layer of doped silicon on a silicon wafer or substrate and depos-

iting a layer of insulating material such as silicon dioxide on the doped silicon. This embodiment includes the use of a silicon on insulator (SOI) substrate. The silicon substrate is adhesive bonded to a glass substrate to create a composite silicon-silicon dioxide-silicon-adhesive-glass structure. The silicon is patterned and etched using anisotropic plasma dry etching techniques. A second patterning then follows to pattern the silicon dioxide layer and an oxygen plasma etch is performed to undercut the adhesive film and to release the doped silicon MEM component. This two-mask process provides single crystal silicon MEM component that is electrically isolated from the glass substrate but mechanically joined thereto.

[0012] The adhesive serves a dual role as a bonding agent and as a sacrificial layer that can be readily removed to release the MEM component in an effective and efficient manner. Specifically, the dry oxygen plasma etch undercuts the adhesive without causing the MEM component to stick to adjacent surfaces — a common problem with wet chemical releases. In addition the oxygen plasma is a benign process with respect to the other material of the composite structure.

[0013] In accordance with the present invention, fabrication of very small cantilever supported beams, switches or other micro electromechanical structures are readily incorporated with other circuit functions on an integrated circuit device. The present invention is particularly well suited for manufacture of long narrow freestanding beams parallel to the substrate that can move in response to pressure, electromagnetic, mechanical or other such stimuli.

[0014] Also, the surfaces of the substrates need not be perfectly smooth since the adhesive layer eliminates the need to use fusion or ionic bonding techniques to form the composite structure. Indeed, pre-existing diffusions or surface irregularities may be present in the substrates with little or no impact on yield or the integrity of the composite structure. This provides very flexible design options since electrical components may be positioned in close proximity to the MEM component.

[0015] These and other advantages of the present invention not specifically described above will become clear within the detailed discussion herein.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0016]

Figure 1 is a sectioned view of the first and second substrates which, when combined, will form a composite structure in accordance with the present invention.

Figure 2 is a sectioned view of the substrates, shown in Figure 1 adhesively bonded to form one embodiment of a composite structure.

Figure 3 is a sectioned view of the composite structure of Figure 2 illustrating a partial etching to define a micro electro-mechanical (MEM) component in accordance with the present invention.

Figure 4 is a sectioned view of the composite structure of Figure 2 illustrating the release of the MEM component in accordance with the present invention.

Figure 5 illustrates, in a general manner, a MEM component manufactured on a glass substrate in accordance with the present invention.

Figure 6 is a sectioned view of another embodiment of a composite structure formed in accordance with the present invention.

Figure 7 shows another alternative embodiment of a composite structure 700 from which a MEM component may be readily obtained.

#### **DETAILED DESCRIPTION OF THE INVENTION**

[0017] In the following description of the preferred embodiment, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and techniques are not shown or discussed in detail in order not to unnecessarily obscure the present invention. Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

[0018] Referring now to Figure 1, process 100 comprises a plurality of steps performed on two principal wafer-like elements: a glass substrate 102 shown with an organic adhesive layer 104 applied to one surface and a sacrificial semiconductor substrate 106. The two substrates are each individually processed, combined to form a composite structure and then further processed to define a micro electro-mechanical (MEM) component.

[0019] MEM components are miniaturized freestanding structures spaced above but physically connected to substrate 102 and electrically coupled to other circuit elements on substrate 102. Examples of typical MEM components may include cantilever supported switches, diaphragms for pressure sensing applications or suspended beams supported at each end but otherwise physically spaced from the substrate.

[0020] Substrate 102 preferably comprises an electri-

cally insulating glass material such quartz, sodium silicate  $\text{Na}_2\text{O-SiO}_2$  or borosilicate  $\text{B}_2\text{O}_3\text{-SiO}_2$ . One preferred substrate uses a high silica glass substrate marketed under the tradename of Vycor, available from Corning Incorporated of Corning, New York. Alternatively, in applications where it is desired to utilize substrate 102 as a conducting element, a semiconductor material may be used. An organic adhesive layer 104 is spun onto substrate 102. Spin coating would provide the most practical method for application of the organic adhesive. However, other coating methods such as spray coating, or staged partially-cured thin films, which are applied to the wafer, by way of example, may be used to deposit organic adhesive layer with substantially uniform thickness.

[0021] Carrier substrate 106 is either a p-type or n-type silicon wafer such as is commonly used in semiconductor processing; the orientation and conductivity of the wafer will, of course, depend on the specific application. Using known semiconductor processing techniques, a silicon layer 108 is grown on carrier substrate 106. Layer 108 may be doped with boron, germanium or other known dopants to impart an etch stop and semiconductor properties. Using semiconductor device manufacturing techniques, electrical components such as resistors, capacitors, inductors or interconnects may be readily formed. An optional silicon dioxide layer 110 is grown on top of silicon layer 108 and an organic adhesive layer 112 is spun on top. The silicon dioxide layer may be eliminated if the rigidity of the MEM component is not critical. Further, either adhesive layer 104 or 112 may be omitted from the process since only one layer may be necessary in some applications.

[0022] The term organic adhesive refers to thermal setting plastics in which a chemical reaction occurs. The chemical reaction increases cross-linking of the polymer to increase rigidity as well as creating a chemical bond with the surfaces being mated.

[0023] While epoxy is the most versatile type of organic adhesive for the present invention, other potential adhesives include polyimide, silicones, acrylics, polyurethanes, polybenzimidazoles and polyquinorolines. Other types of organic adhesives such as thermal plastics, which require heating above their melting point like wax, would not be of value for this application. The selection of the adhesive would depend in large part on the polymer's thermal characteristics and particularly its glass transition temperature. Other selection criteria include economics, adhesive strength on different substrates, cure shrinkage, environmental compatibility and coefficient of thermal expansion.

[0024] The glass transition temperature is the temperature at which chemical bonds can freely rotate around the central polymer chain. As a result, below the glass transition temperature, the polymer, when cured, is a rigid glass-like material. Above the glass transition, however, the polymer is a softer elastomeric material. Further at the glass transition temperature, there is a

substantial increase in the coefficient of thermal expansion (CTE). Accordingly, when the glass transition temperature is exceeded, there is an increase in the CTE and there is a relief of stress in the polymer layer.

[0025] Substrates 102 and 106 may be treated to improve the adhesion of the epoxy. Common treatments include plasma or surface etch treatments. The use of a coupling agent or adhesion promoter such as 3-glycidyloxypropyl-tri-methoxy-silane (available from Dow Corning as Z-6040) or other agents having long hydrocarbon chains to which the epoxy may adhere may be used to improve coating consistency. Wetting agents may be used to improve coating uniformity. However, in most cases, the coupling agent may serve dual purposes of surface wetting and surface modification. With the use of organic material, surface finish is not overly critical and the surface need not be smooth. Surface structures such as resistors, inductors, capacitors, transistors or conductors may advantageously be added to the surface areas of substrates 102 and 106.

[0026] Substrates 102 and 106 are then positioned in a vacuum chamber (not shown) with opposing adhesive layers 104 and 112. The chamber is evacuated to remove air that could be trapped between the substrates during the mating process. Once a vacuum is achieved, the substrates are aligned and physically joined together to form a composite structure with a single bead of epoxy. Advantageously, backside alignment marks may be optically referenced to facilitate the alignment.

[0027] Composite structure 200 is shown more clearly in Figure 2. The organic adhesive layers 104 and 112 combine to form a single adhesive layer 202 to bond the composite structure. The adhesive is cured by baking composite structure 200 for a sequence of oven bakes at elevated temperatures of up to 180 °C to reduce cure shrinkage. The recommended cure temperatures depend on the type of epoxy used. Preferably) once cured, the epoxy is able to withstand elevated temperatures typically associated with many semiconductor processing steps (that is, a temperature up to 250°C) without additional shrinkage or substantial degradation.

[0028] Further) the adhesive should have a limited amount of cure shrinkage so as to minimize the possibility of inducing cracking or stress fractures in composite structure 200. The phrase "cure shrinkage" refers to a change in volume of a thermosetting adhesive during the cure cycle due to the reaction, generally an out-gassing product or rearrangement of the polymer itself. Cure shrinkage can cause considerable pressure to develop along the length of the bond during processing.

[0029] An additional component closely associated with cure shrinkage is the adhesive's CTE at the cure temperature and at the operating temperature. Generally, organic adhesives will have a higher CTE than any other material present in the MEM component. This means that the adhesive will expand at a higher rate than will other material as the ambient temperature

increases. Although an inorganic filler material may be added to the adhesive to reduce the CTE such fillers are not recommended in this application since such inorganic filler material cannot be etched using oxygen plasma during the structural releasing step.

[0030] Substrate 102 may also be selected for a desired CTE. The substrate in one preferred embodiment has a CTE that is substantially similar to but less than that of silicon so that the resulting MEM component will be slightly stretched (or in tension). In this manner, smaller structures will retain some degree of elasticity and will be less susceptible to developing a bow or collapsing upon release of the MEM component. It will be appreciated that if the CTE of substrate 102 is greater than that of silicon, the MEM component will be in compression upon release. Larger beams may be capable of retaining the structural integrity in compression after all process steps are complete. Use of glass substrate 102 was selected in the described embodiment primarily to achieve high electrical isolation. However, one skilled in the art will appreciate that the process steps of the present invention may be applied to selected substrates other than the above described glass substrate due to the versatility of the bonding and sacrificial layer.

[0031] Due to the number of material types present in the composite structure 200, thermal processing and the mismatching of thermal coefficients may impart shear fractures or stress cracks in one or both substrates or in the various layers. The CTE in the bond line of the MEM component will depend upon the polymer used, its curing agent, and the thermal cycle used to cure the polymer. When the processing and operating temperatures are maintained so that the polymer is not exposed to temperatures exceeding the glass transition temperature, the polymer is a rigid glass-like material and the CTE is minimized. If the glass transition temperature is exceeded, however, there will be an increase in the CTE, which may result in a relief of stress in the polymer layer. Any such stress relief after composite structure 200 is formed may deform composite structure 200. Since flexible or elastomeric polymers will have a high CTE, a thin bond line is desirable to minimize structural damage in the event the glass transition temperature is inadvertently exceeded. In one preferred embodiment, the bond line has a thickness of about five (5) to seven (7) microns.

[0032] Referring again to Figure 1, the next step is to remove substrate 106 and expose silicon layer 108. Substrate 106 is removed using a backside chemical etch. A mechanical grinding or polishing step may proceed the chemical etch to reduce the amount of silicon etching required or to reduce the selectivity needed in the etch step. Since substrate 106 primarily functions as a sacrificial carrier for silicon layer 108, there is no need to preserve substrate 106 in the region of the MEM component so as to facilitate subsequent processing of silicon layer 108. Alternatively, if a specific application required thick or rigid beams, one skilled in the art will

appreciate that substrate 106 could be patterned and selectively etched for use as beam material or retained in adjacent areas as a substrate for integrated circuit devices.

[0033] As shown in Figure 3, an optional layer of aluminum 116 is deposited onto the exposed surface of silicon layer 108. Aluminum 116 is patterned with a first mask to form conducting areas and to expose selected portions of silicon layer 108. The aluminum is either lifted off or etched using an aluminum-specific chemical agent. Although not shown, an oxide or nitride cap may be applied on top of the aluminum layer 116 to form a protective barrier.

[0034] With silicon layer 108 exposed through the aluminum 116, an anisotropic etch defines the structural dimensions of the MEM component. This etch stops upon reaching the silicon dioxide layer 110.

[0035] A second mask is applied to pattern the insulating silicon dioxide layer 110 and then etched. It is important to note that due to its insulating properties, portions of silicon dioxide layer 110 may be retained to mechanically support selective areas of the MEM component while maintaining electrical isolation. Specifically as shown in Figure 5, holes 150 may be etched into silicon dioxide layer 110 to facilitate etching adhesive layer 120.

[0036] Referring now to Figure 4, adhesive layer 120 is etched in a final process step to release the MEM component. In the preferred embodiment, dry oxygen (O<sub>2</sub>) plasma etch undercuts adhesive layer 120. Since this plasma etch is a dry release, manufacturing yields are improved relative to wet etching. Specifically, as one familiar with semiconductor technology will appreciate, wet etching may lower production yields as water molecules get trapped under the released MEM components causing the MEM component to stick to substrate 102.

[0037] Upon MEM component release, stress forces along the bond line will be substantially released. Further, any pressure generated by shrinkage of the organic adhesive during cure will be significantly reduced after processing by dicing the wafers into discrete devices resulting in mechanically stable devices.

[0038] Another embodiment of a composite structure formed in accordance with the present invention is shown in Figure 6. Structure 600 comprises a first and second substrate 106 and 102. Specifically, substrate 102 is preferably a glass substrate that exhibits high electrical isolation while substrate 106 is a semiconductor substrate. Substrate 106 may be either p or n-type and may be selectively doped to impart conductive or semiconductor properties. Substrates 102 and 106 are joined together by an adhesive film 602.

[0039] If preferred, substrate 106 may be ground and polished to a desired thickness, patterned to define a MEM component and etched to expose the adhesive film 602. The film is then patterned and dry etched to release the MEM component. As will be understood, substrates 102 and 106 may further include conductive

elements such as switch contacts or electrodes (not shown).

[0040] Figure 7 shows another alternative embodiment of a composite structure 700 from which a MEM component may be readily obtained. Silicon on insulator (SOI) substrate 702 has a buried layer of silicon dioxide layer 704 that acts as an etch stop. The buried silicon dioxide layer can be formed by several commercially available techniques, including implanting oxygen (O<sub>2</sub>), deep into substrate 702. The silicon-oxide-silicon (which may be either doped to impart semiconductor properties or undoped) is adhesively bonded to substrate 706 to form a composite structure. In the preferred embodiment, substrate 706 is a glass substrate. Using the techniques described above, the MEM component is defined and released by the two-mask patterning and etching process.

[0041] Referring again to Figure 5, a topological view of an integrated circuit comprising a MEM component is shown. This circuit is an exemplary view of one type of MEM component that may be created using the process of the present invention. Beams 152 of about one micrometer wide and several millimeters in length are constructed using the above-described process. The thickness of these beams may range from about 20-30 micrometers up to about 100 micrometer. One skilled in the art will appreciate that the above-described dimensions may be readily changed depending on the specific application. Support beams 154 may add rigidity to selected ones of beams 152.

[0042] With the present invention a very high aspect ratio may be achieved for the MEM component. By way of example, very narrow, deep MEM sensors are obtained using the above described process steps. Thus this type of sensor will have high capacitance value that is easy to detect. Advantageously, sensor interface may be achieved by electrically bonding to pads 156.

[0043] The process of the present invention is independent of the substrate material. Since epoxy or organic adhesives, in general, readily bond a wide variety of substrates, substrates may be selected depending on the specific application in which the MEM component will interface. The low temperature bonding readily enables the use of gallium arsenide, silicon or other material on a glass substrate. Further, the process is readily applied to applications where silicon or gallium arsenide substrates are desired instead of a glass substrate.

[0044] It will be appreciated that it is also very desirable in many applications to position electronic circuits in close proximity to the MEM component. With the present invention, transistors or other circuit elements may be fabricated directly on the silicon, prior to creating the composite structure of Figure 2. Further, with the present invention, structures can be formed on both sides of the beam. By way of example, aluminum can be deposited between the silicon dioxide and the silicon

layers (see Figure 1) to create a very conductive structure. One skilled in the art will appreciate that the low process temperatures employed to create the composite structure, to define or to release the MEM components has minimal impact on junction depths or circuit device parameters.

[0045] While certain exemplary preferred embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention. Further, it is to be understood that this invention shall not be limited to the specific construction and arrangements shown and described since various modifications or changes may occur to those of ordinary skill in the art without departing from the spirit and scope of the invention as claimed.

[0046] The present invention relates to a fabrication process relating to a fabrication process for manufacture of micro-electromechanical (MEM) devices such as cantilever supported beams. This fabrication process requires only two lithographic masking steps and offers moveable electromechanical devices with high electrical isolation. A preferred embodiment of the process uses electrically insulating glass substrate as the carrier substrate and single crystal silicon as the MEM component material.

[0047] The process further includes deposition of an optional layer of insulating material such as silicon dioxide on top of a layer of doped silicon grown on a silicon substrate. The silicon dioxide is epoxy bonded to the glass substrate to create a silicon-silicon dioxide-epoxy-glass structure. The silicon is patterned using anisotropic plasma dry etching techniques. A second patterning then follows to pattern the silicon dioxide layer and an oxygen plasma etch is performed to undercut the epoxy film and to release the silicon MEM component. This two-mask process provides single crystal silicon MEMs with electrically isolated MEM component. Retaining silicon dioxide insulating material in selected areas mechanically supports the MEM component.

## Claims

1. A method for fabricating a micro electromechanical (MEM) component on a substrate comprising the steps of:

Providing a first substrate (106, 108);  
 Providing a second substrate (102);  
 Adhesively bonding (at 120) said first substrate (106, 108) to said second substrate (102) to form a composite structure (200);  
 Patterning and etching said first substrate (106, 108) to define a MEM component; and  
 Patterning and etching said adhesive bond (120) to release said MEM component.

2. The method of claim 1 further comprising the step

of reducing the thickness of said first substrate (106, 108) prior to the first of said patterning and etching steps.

3. A method for fabricating a micro electromechanical (MEM) component on a substrate comprising the steps of:

Providing a first substrate (106);  
 Providing a first layer of material (108) on said first substrate (106);  
 Providing a second substrate (102);  
 Adhesively bonding (at 120) said first layer of material (108) to said second substrate (102) to form a composite structure (200);  
 Patterning and etching said first substrate (106) to expose said first layer of material (108);  
 Patterning and etching said first layer of material (108) to define a MEM component; and  
 Etching said adhesive bond (120) to release said MEM component.

4. The method of any preceding claim further comprising the step of doping said first substrate (106, 108) or said first layer of material (108), respectively, to impart etch stop and/or semiconductor properties thereto.

5. The method of claim 3 or 4 wherein said etching of said adhesive bond (120) comprises the step of performing an oxygen plasma etch to selectively undercut and to release the MEM component while maintaining said composite structure.

6. The method of any of claims 3 to 5 further comprising the steps of growing a silicon dioxide layer (110) on top of said first layer of material (108) and depositing a layer of organic adhesive (112) on top of said silicon dioxide layer (110).

7. The method of any of claims 3 to 5 wherein said bonding step further comprises the step of:

Depositing a layer of organic adhesive (104, 112) on at least one of said second substrate (102) and said first layer of material (108) with a layer of epoxy;  
 Positioning said first and second substrate (106 and 102) in a vacuum chamber with said adhesive layer (104, 112) there-between;  
 Evacuating the air in said chamber;  
 Joining together said first and second substrate so as to form a single epoxy bond (120) there-between; and  
 Curing said epoxy.

8. A method for fabricating a micro electromechanical

component on a substrate comprising the steps of:

Providing a silicon substrate (106);  
 Depositing a layer of semiconductor material (108) on said silicon substrate (106);  
 Providing a highly insulating substrate (102);  
 Bonding said highly insulating substrate to said semiconductor material to form a composite structure (200);  
 Patterning and etching said silicon substrate (106) to expose said semiconductor material (108);  
 Patterning and etching said semiconductor material (108) to define a micro electromechanical component; and  
 Performing an isotropic etch to selectively undercut the bond (120) and to release said micro electromechanical component.

9. The method of claim 3 or 8 wherein said etching of said first substrate (106) or said silicon substrate (106), respectively, comprises the step of performing an anisotropic plasma dry etch.

10. The method of claims 8 or 9 further comprising the steps of growing a silicon dioxide layer (110) on top of said semiconductor material (108);

preferably further comprising a step of depositing a layer of organic adhesive (112, 104) on top of at least one of said silicon dioxide layer (110) and said insulating substrate (102) prior to said bonding step; and  
 wherein said etching of said adhesive bond step preferably comprises the step of performing an isotropic etch to selectively undercut said bond (120) and to release the micro electromechanical component while maintaining said composite structure (200).

11. The method of claim 8 or 9 wherein said bonding step further comprises the step of:

Depositing a layer of organic adhesive (104, 112) on one side of said at least one of said semiconductor material (108) and said highly insulating substrate (102);  
 Positioning said first and second substrate (106 and 102) in a vacuum chamber with said adhesive layer (104, 112) there-between;  
 Evacuating the air in said chamber;  
 Placing said first and second substrates into physical contact so as to form a single adhesive bond (120) there-between; and  
 Curing said adhesive.

12. The method as claimed in any of claims 8 to 11 further comprising the step of providing a

- plurality of electronic elements in close proximity to said micro electromechanical component on said highly insulating substrate (102); wherein said providing step preferably comprises the step of fabricating transistors or other circuit elements directly in semiconductor material prior to said bonding step; and wherein said providing step preferably comprises the step of fabricating circuit elements on said semiconductor material (108) after said etching step to remove said first substrate (106) so as to provide circuit elements on the side of said micro electromechanical component facing away from said highly insulating substrate (102) where said circuit elements comprise resistors, capacitors, inductors and interconnects.
13. A method for fabricating a micro electromechanical component on a substrate comprising the steps of:
- Providing a silicon-on-insulator (SOI) substrate (702) having a buried layer of insulating material (704);
- Providing a highly insulating substrate (706);
- Bonding said highly insulating substrate (706) to said SOI substrate (702) to form a composite structure (700);
- Patterning and etching said SOI substrate (702) to expose said buried layer insulating material (704);
- Patterning and etching said buried layer insulating material (704) to define a micro electromechanical component; and
- Selectively etching to undercut the bond under said micro electromechanical component so as to release the micro electromechanical component.
14. The method of claim 3, 8 or 13 wherein said second substrate (102) or said highly insulating substrate (102, 706), respectively, comprises a glass substrate, preferably a highly insulating glass substrate.
15. The method of claim 3, 4 or 14 wherein said etching of said first substrate (106) or said SOI substrate (702), respectively, comprises the step of performing an anisotropic plasma dry etch.
16. The method of claim 15 further comprising the step of depositing a layer of organic adhesive on said SOI substrate (702) prior to said bonding step.
17. The method of claim 3, 8 or 13 wherein said bond is an adhesive bond made by an organic adhesive selected from the following: epoxy, polyimide, silicone, acrylic, polyurethane, polybenzimidazole and polyquinoraline; and preferably further comprising the step of depositing a conductive layer of metal (116) on top of said composite structure (200; 700) after said patterning and etching of said silicon substrate step or said SOI substrate step.
18. The method of claim 17 wherein said etch process step to release the MEM component from said bond (120) comprises an oxygen plasma etch.
19. The method of claims 8 to 10 or claim 17 wherein said bonding step further comprises the step of:
- Positioning said substrate with at least one said adhesive layer (112, 104) there-between;
- Evacuating the air between said substrates;
- Placing said substrates into physical contact to form a single adhesive bond, for example epoxy bond (120), thereby forming a composite structure (200; 700); and
- Curing said adhesive.
20. The method of any of claims 3 to 6, 8 to 11, 13 to 19, wherein said organic adhesive bond or said adhesive bond, respectively, is epoxy.
21. In a semiconductor device, a composite structure comprising:
- a first substrate (106) having a first layer of material (108) on said first substrate;
- a second substrate (102) adhesively bonded (at 120) to said first layer of material (108) to form a composite structure (200), and
- a micro electromechanical (MEM) component formed in said first layer of material (108) and having said first substrate (106) removed therefrom, said MEM component being separated from said second substrate (102) by a dimension substantially equal to the dimension of said adhesive bond (120).
22. The composite structure of claim 21 wherein said first substrate (106) is substantially completely removed from said first layer of material (108) and said composite structure further comprises:
- a layer of conductive material (116) deposited on top of said first layer (108); and
- a protective barrier layer (110).
23. The composite structure of claim 21 wherein:
- said first layer of material (108) comprises material exhibiting semiconductor properties;



said composite structure (200) preferably further comprises a protective barrier layer (110) between said first layer of material (108) and said adhesive bond layer (120); and wherein said second substrate (102) preferably 5  
comprises a substrate having high electrical isolation properties.

24. In a semiconductor device, a composite structure comprising: 10

a first substrate (106, 108);  
a second substrate (102) adhesively bonded (at 120) to said first substrate (106, 108) to form a composite structure (200), and 15  
a micro electromechanical (MEM) component formed in said first substrate (106, 108), said MEM component being separated from said second substrate (102) by a dimension substantially equal to the dimension of said adhesive bond (120). 20

25. The composite structure of claim 24 wherein the thickness of said first substrate defines said MEM component, said first substrate further comprises: 25

a layer of conductive material (116); and  
a protective barrier layer (110);  
said first substrate (106, 108) preferably comprising material exhibiting semiconductor properties and said second substrate (102) preferably comprising material exhibiting high electrical isolation. 30

26. The composite structure of claim 24 wherein said composite structure (200) further comprises a protective barrier layer (110) between said first layer of material (108) and said adhesive bond layer (120). 35

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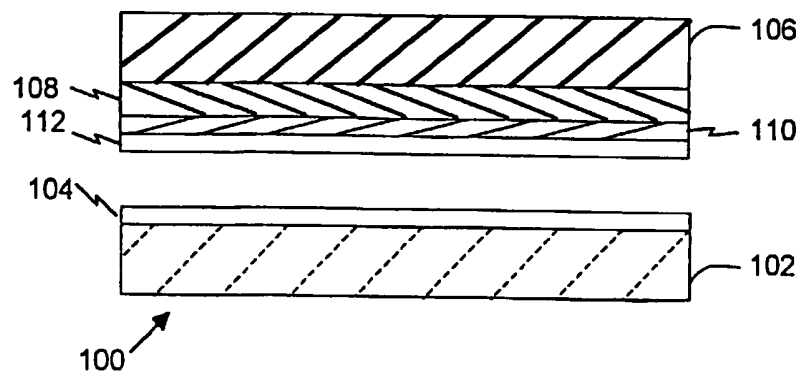


Figure 1

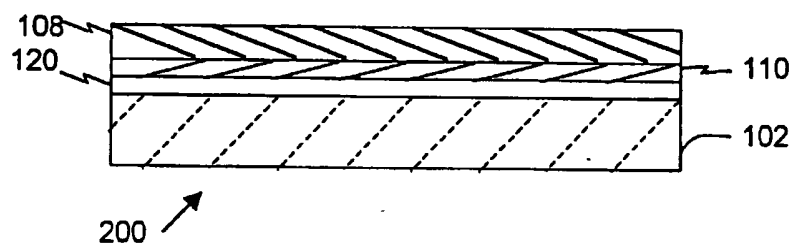


Figure 2

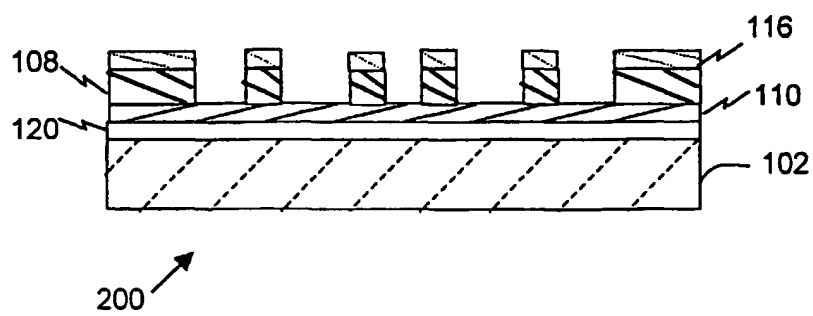


FIGURE 3

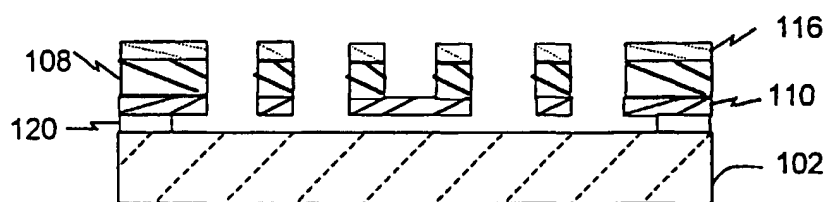


FIGURE 4

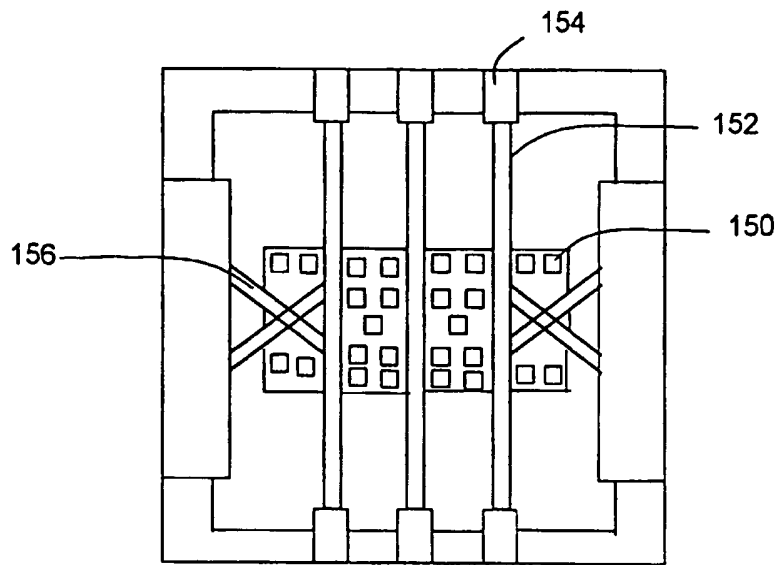


Figure 5

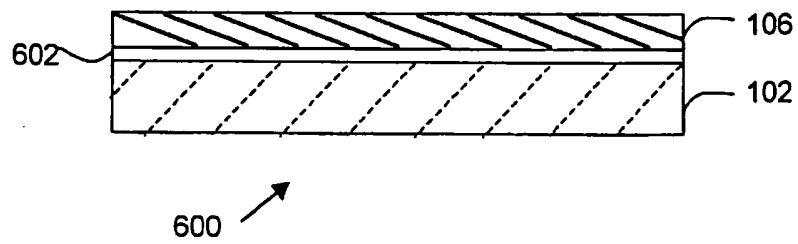


Figure 6

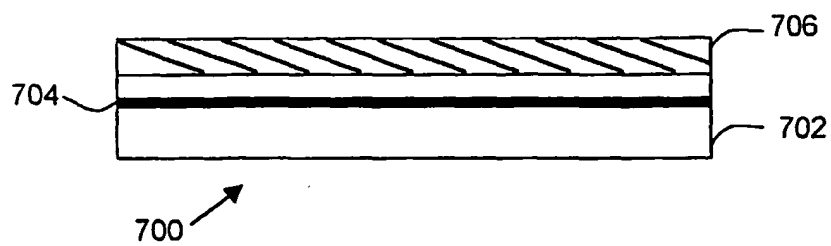


Figure 7

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